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June 15, 2000

Attorney Docket No.: 08305/073001/99-08/99-09/99-10

Box Patent Application

Commissioner for Patents
Washington, DC 20231

Presented for filing is a new patent application claiming priority from a provisional patent application of:

Applicant: ANDERS ANDERSSON

Title: ACTIVE PIXEL SENSOR (APS) READOUT STRUCTURE WITH
AMPLIFICATION

Enclosed are the following papers, including those required to receive a filing date under 37 CFR 1.53(b):

	<u>Pages</u>
Specification	10
Claims	5
Abstract	1
Declaration	2
Drawing(s)	7

Enclosures:

- Assignment cover sheet and an assignment, 2 pages, and a separate \$40 fee.
- Small entity statement. This application is entitled to small entity status.
- Postcard.

Under 35 USC §119(e)(1), this application claims the benefit of prior U.S. provisional application 60/139,348, filed June 15, 1999.

CERTIFICATE OF MAILING BY EXPRESS MAIL

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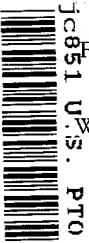
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Frederick P. Fish
1855-1930

W.K. Richardson
1859-1951



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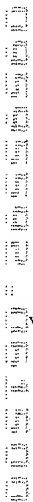
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Page 2

There are 17 claims, 2 independent.

Basic filing fee	\$345
Total claims in excess of 20 times \$9	\$0
Independent claims in excess of 3 times \$39	\$0
Fee for multiple dependent claims	\$0
Total filing fee:	\$345

A check for the filing fee is enclosed. Please apply any other required fees or any credits to deposit account 06-1050, referencing the attorney docket number shown above.

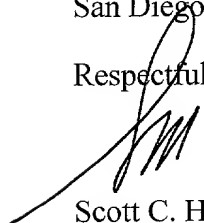
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Kindly acknowledge receipt of this application by returning the enclosed postcard.

Please send all correspondence to:

SCOTT C. HARRIS
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Respectfully submitted,



Scott C. Harris
Reg. No. 32,030
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ATTORNEY DOCKET NO. 08305-073001

Applicant or Patentee: Anders Andersson

Serial or Patent No.: _____

Filed or Issued: _____

For: ACTIVE PIXEL SENSOR (APS) READOUT STRUCTURE WITH AMPLIFICATION**VERIFIED STATEMENT (DECLARATION) CLAIMING SMALL ENTITY STATUS
(37 CFR 1.9(f) and 1.27(c)) — SMALL BUSINESS CONCERN**

I hereby declare that I am

- ☐ the owner of the small business concern identified below:
☒ an official of the small business concern empowered to act on behalf of the concern identified below:

Name of Small Business Concern: PHOTOBIT CORPORATIONAddress of Small Business Concern: 135 North Los Robles Avenue, 7th Floor
Pasadena, California 91101

I hereby declare that the above identified small business concern qualifies as a small business concern as defined in 13 CFR 121.802, and reproduced in 37 CFR 1.9(d), for purposes of paying reduced fees to the United States Patent and Trademark Office, in that the number of employees of the concern, including those of its affiliates, does not exceed 500 persons. For purposes of this statement, (1) the number of employees of the business concern is the average over the previous fiscal year of the concern of the persons employed on a full-time, part-time or temporary basis during each of the pay periods of the fiscal year, and (2) concerns are affiliates of each other when either, directly or indirectly, one concern controls or has the power to control the other, or a third party or parties controls or has the power to control both.

I hereby declare that rights under contract or law have been conveyed to and remain with the small business concern identified above with regard to the invention, entitled **ACTIVE PIXEL SENSOR (APS) READOUT STRUCTURE WITH AMPLIFICATION** by inventor(s) **ANDERS ANDERSSON** described in:

- ☒ the specification filed herewith.
☐ application serial no. filed .
☐ patent no. issued .

If the rights held by the above identified small business concern are not exclusive, each individual, concern or organization having rights to the invention is listed below* and no rights to the invention are held by any person, other than the inventor, who would not qualify as an independent inventor under 37 CFR 1.9(c) if that person made the invention, or by any concern which would not qualify as a small business concern under 37 CFR 1.9(d), or a nonprofit organization under 37 CFR 1.9(e). *NOTE: Separate verified statements are required from each named person, concern or organization having rights to the invention averring to their status as small entities. (37 CFR 1.27)

Full Name: _____

Address: _____

☐ INDIVIDUAL ☐ SMALL BUSINESS CONCERN ☐ NONPROFIT ORGANIZATION

I acknowledge the duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status when any new rule 53 application is filed or prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate. (37 CFR 1.28(b))

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent on which this verified statement is directed.

Name:	<u>Angela L. McNamee</u>
Title:	<u>Secretary</u>
Address:	<u>135 North Los Robles Avenue, 7th Floor Pasadena, California 91101</u>

Signature: Angela L. McNameeDate: 6/15/00

APPLICATION
FOR
UNITED STATES LETTERS PATENT

TITLE: ACTIVE PIXEL SENSOR (APS) READOUT STRUCTURE
WITH AMPLIFICATION

APPLICANT: ANDERS ANDERSSON

CERTIFICATE OF MAILING BY EXPRESS MAIL

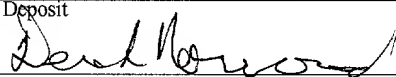
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Derek Norwood

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ACTIVE PIXEL SENSOR (APS) READOUT STRUCTURE WITH AMPLIFICATION

CROSS REFERENCE TO RELATED APPLICATION

This application claims the benefit of the U.S.
Provisional Application No. 60/139,348 entitled NOVEL IDEA FOR
5 A NEW READOUT STRUCTURE OF APS filed on June 15, 1999.

BACKGROUND

Active pixel sensor (APS) imaging devices are described
in U.S. Patent No. 5,471,515. These imaging devices include
an array of pixel cells that convert light energy into
10 electrical signals. Each pixel includes a photodetector and
one or more active transistors formed of MOS technology. The
transistors typically provide amplification, readout control
and reset control, in addition to producing the electrical
signal output from the cell.

15 APS devices may be fabricating using CMOS technology. An
APS sensor, including a pixel array and readout structure, may
be provided on the same integrated circuit (IC) chip. The
gain stage of the APS sensor may consume a considerable amount
of the chip area. However, reducing the size of this area may
20 sacrifice signal gain in the APS sensor.

The readout structure of an APS typically includes a
source follower transistor. Use of such a transistor may

itself limit the dynamic range of the sensor when reading out the pixel and provide a voltage gain less than unity.

SUMMARY

An active pixel sensor (APS) according to an embodiment includes an array of individually addressable APS cells, each of which include a row select transistor and an output transistor, and a pixel readout structure that includes an amplifier. The amplifier structure includes the row select transistor and output transistor of each pixel. The amplifier may provide a gain of one or higher.

According to an embodiment, the amplifier has a two branched structure. One branch includes a transistor connected to V_{DD} , and the output transistor and the row select transistor for each pixel in a column. The other branch includes three transistors in series, the first connected to V_{DD} , and the third connected to the drain of a source follower transistor connected to ground. The row select transistor for each pixel in the column is also connected to the source follower transistor. The transistors in the branches connected to V_{DD} may be p-type MOSFETS and the other transistors may be n-type MOSFETS.

According to another embodiment, a transistor may be connected between the pixel output transistor and the p-type

transistor in each pixel to protect the output transistor from voltage charges in the column line.

According to another embodiment, the amplifier may be provided with a gain selector to optionally change the gain in the amplifier. The gain selector may comprise two p-type transistors connected between the source of the p-type transistor in each branch and V_{DD} : a gain transistor and a gain-enable transistor. The gain transistor, connected to V_{DD} , may be self-biased, and the gain-enable transistor may be controlled between ON and OFF states by a gain voltage source. When the gain-enable transistor is ON, the gain transistor and other transistor at V_{DD} are effectively in parallel, thereby altering the gain of the amplifier.

The details of one or more embodiments of the invention are set forth in the accompanying drawings and the description below. Other features, objects, and advantages of the invention will be apparent from the description and drawings, and from the claims.

DESCRIPTION OF DRAWINGS

FIG. 1 is a schematic diagram of an active pixel sensor (APS) including an amplifier circuit in the readout structure according to an embodiment.

FIG. 2 is a schematic diagram of an amplifier according to the embodiment of FIG. 1.

FIG. 3 is a schematic diagram of an APS according to another embodiment.

5 FIG. 4 is a graph illustrating an input signal for a simulation performed on the embodiment of FIG. 3.

FIG. 5 is a graph illustrating a response of the embodiment of FIG. 3 with the input of FIG. 4.

10 FIG. 6 is a schematic diagram of an APS according to another embodiment including voltage protection for the pixel output transistors.

FIG. 7 is a schematic diagram of an APS according to another embodiment including a gain selector in the amplifier.

15 Like reference symbols in the various drawings indicate like elements.

DETAILED DESCRIPTION

20 An embodiment is shown in FIG. 1. The readout structure 102 of an active pixel sensor (APS) 100 includes an amplifier circuit 104. The APS includes an array 106 of independently addressable pixels arranged in n rows and m columns. FIG. 1 illustrates two of the pixels 108, 110 that are connected to a column of line 112 of the pixel array. Pixel 108 is in row 1 and pixel 110 is in row 2. Each pixel includes a

photodetector 114, such as a photogate, photodiode or pinned photodiode, a reset transistor 116, a source-follower output transistor 118 (denoted M1), and a row select transistor 120 (denoted M6). The gate 122 of the output transistor is

5 connected to a pixel voltage provided by the photodetector.

The gate 124 of the row select transistor 120 is connected to a row enable voltage which is set HIGH when the pixel is being read out, thereby allowing the voltage on the output

transistor to be passed to the column line 112. The output transistor 118 and row select transistors 120 may be n-type MOSFET transistors.

The drain 130 of each output transistor 118 in the column is connected to the source 132 of a p-type transistor 134 (denoted M3). The drain 136 of transistor 134 is connected to a system drain voltage V_{DD} , and the gate 138 of transistor 134 is connected to its source. The source of each row select transistor 120 in the column is connected to the drain 140 of an n-type source follower transistor 142, which has a gate 144 connected to a bias voltage, V_{bias} , and a source 146 connected to ground.

When a pixel is being read out, the p-type transistor 134, pixel output transistor 118, and pixel row enable transistor 120 form one branch of the amplifier circuit 104. A second branch of the amplifier circuit includes a p-type

transistor 150 (denoted M4) and two n-type transistors 152, 154 (denoted M2 and M7, respectively). The drain 156 of p-type transistor 150 may be connected to V_{DD} and its gate 158 connected to its source 160. The drain of transistor 152 is connected to the source of transistor 150 and the gate 162 is connected to a load voltage V_n . The drain of transistor 154 is connected to the source of transistor 152, its gate 164 is connected to V_{DD} and its source is connected to the drain of source-follower transistor 142. Transistor 154 in the second branch may be provided for symmetry with row enable transistor 120 in the pixel being read out.

When the pixel is read out, the row enable voltage is set HIGH, and row select transistor 120 and transistor 154 are essentially shorted out. The relationship of the remaining transistors in the amplifier circuit 104 may be described as shown in FIG. 2. The gain of the amplifier is:

$$(1) \quad A_0 = g_{m1} * (r_{ds2} // r_{s4}) = // r_{ds2} \gg r_{s4} // \approx g_{m1} * r_{s4} = g_{m1} / g_{m4} = // \mu_n \approx 3 * \mu_p // \approx (3 * (W/L)_1 / (W/L)_4)^{1/2}$$

When V_p equals V_n the output is the same and these outputs are:

$$(2) \quad V_{out+} = V_{out-} = V_{DD} - V_{gs4} = V_{DD} - V_{eff-} - |V_{tp}| = V_{DD} - (I_{bias} / \mu_p * C_{ox} * (W/L)_4)^{1/2} - |V_{tp}|$$

A simple first order transfer function of a dominant pole op amp can be described by:

$$(3) \quad A_v(s) = A_0 / (1 + s/\omega)$$

(4) $A_v(s) = g_{m1} * (r_{out} // 1/sC_L) =$ for midband frequencies C_L dominates $= g_{m1}/sC_L => |A_v(j\omega_{ta})| = 1 =>$

(5) $\omega_{ta} = g_{m1}/C_L => \omega < \omega_{ta};$ and

(6) $A_0 * \omega = \omega_{ta} = g_{m1}/C_L =>$

5 (7) $t_{switch} \cong C_L * A_0 / g_{m1}$, where

G_m is the transistor's transconductance,

R_{ds} is the Drain-Source resistance,

R_s is the source resistance,

C_{ox} is the gate oxide,

10 V_{gs} is the Gate-Source voltage,

V_{tp} is the threshold voltage for PMOS,

W is the channel width,

L is the channel length,

μ_n is the mobility of the NMOS transistor,

15 μ_p is the mobility of the PMOS transistor, and

the subscripted numerals refer to the transistor denotations.

Typical values in a 0.8 μm -process are:

$|V_{tp}| = |V_{tn}| = 0.8V;$ and

20 $\mu_n * C_{ox} \approx 3 * \mu_p * C_{ox} \approx 90 \mu A/V.$

The dimensions of the various transistors may be adjusted to reduce noise. For example, the length of transistor 150 (M4) may be decreased to decrease flicker noise. Input noise may be independent of the width of transistor 150. That width

hence may be widened to maximize signal swing at the output. Also, increasing the length of the pixel output transistor 118 may increase noise, whereas increasing the width of the transistor 118 may reduce flicker noise, thermal noise, and white noise.

The gain of the amplifier 104 according to the embodiment may be set to unity or higher. The response of a simulated sensor according to the embodiment shown in FIG. 3 was demonstrated with a gain value set to four (4). The simulation included three pixels, each with a pixel voltage, V_{in+1} , V_{in+2} , and V_{in+3} , respectively. The potentials used in the simulation were as follows: $V_{DD} = 5$ V; $V_{in-} = 2.85$ V; $V_{in+1} = 3.3$ V; $V_{in+2} = 2.7$ V; and $V_{bias} = 1.2$ V. V_{in+3} 400 was varied as shown in FIG. 4. FIG. 5 illustrates the voltage response 500 of the simulated sensor. The sensor including the amplifier in the readout structure demonstrated a relatively higher dynamic range and gain than expected from a source follower transistor alone.

According to an embodiment shown in FIG. 6, another transistor 600 (denoted M8) may be provided in the pixel between the p-type transistor and pixel output transistor. This blocking transistor may protect the output transistor from being effected by voltage changes in the branch line 135 when reading other pixels in the column.

FIG. 7 shows an embodiment with additional structure added to the amplifier circuit to enable the selection of different gain settings for the amplifier. Another self-biased p-type transistor, gain transistor 700, is added to each branch between V_{DD} and a node 702 at the sources of the p-type transistors 134, 150. A gain-enabled p-type transistor 704 is connected between the node 702 and the source of the gain transistor 700. The gate of each gain-enabled transistor 704 is connected to a variable gain voltage, V_{gain} . When V_{gain} is set HIGH, the gain-enabled transistor 704 is OFF and the circuit operates similarly to the embodiment shown in FIG. 1. To alter the gain provided by the amplifier, V_{gain} may be set to LOW, turning the gain-enabled transistor 704 ON and effectively placing p-type transistor 134, 150 (M3, M4) and the respective gain transistor 700 in each branch in parallel. Thus, the effective source resistance of the p-type transistors 134, 150 will decrease. As may be determined from equation (1), this will increase the gain of the amplifier as gain is inversely proportional to the source resistance of the p-type transistors 134, 150.

The branched amplifier according to an embodiment may reduce noise from the substrate because it provides a differential output. The amplifier may also improve the dynamic range of the sensor when reading out a pixel because

loss from the source follower may be reduced with the addition
amplifier structure.

A number of embodiments of the invention have been
described. Nevertheless, it will be understood that various
5 modifications may be made without departing from the spirit
and scope of the invention. Accordingly, other embodiments
are within the scope of the following claims.

WHAT IS CLAIMED IS:

1 1. An imaging device comprising:

2 a plurality of active pixel sensor cells, each
3 having a photosensor, a row select transistor, and an output
4 transistor including a gate connected to a pixel output
5 voltage; and

6 a readout circuit connectable to each of said APS
7 cells, said readout circuit including an amplifier, said
8 amplifier including the row select transistor and the output
9 transistor of each of a plurality of said active pixel sensor
10 cells.

1 2. The imaging device of claim 1, wherein the amplifier
2 provides a gain of about one or higher.

1 3. The imaging device of claim 1, wherein the amplifier
2 comprises:

3 a first branch comprising:

4 a first transistor having a drain connected to
5 a first voltage source;

6 the row select transistor of each pixel; and

7 the output transistor of each pixel;

8 a second branch comprising:

9 a second transistor having a drain connected to
10 the first voltage source;

11 a third transistor having a gate connected to a
12 second voltage source; and

13 a source follower transistor having a drain
14 connected to a source of each of the third
15 transistor and the output transistor of each pixel.

1 4. The imaging device of claim 3, wherein the first
2 voltage source comprises V_{DD} .

1 5. The imaging device of claim 3, wherein each of the
2 first and second transistors comprise a p-type transistor and
3 each of the row select transistors, output transistors, third
4 transistor, and source follower transistor comprise an n-type
5 transistor.

1 6. The imaging device of claim 3, further comprising a
2 fourth transistor connected between the third transistor and
3 the source follower transistor, said fourth transistor
4 comprising a gate connected to the first voltage source.

1 7. The imaging device of claim 3, wherein each pixel
2 and the amplifier are connected to a column line, and further

3 comprising a switch in each pixel to shield the output
4 transistor from voltage changes in the column line.

1 8. The imaging device of claim 7, wherein the switch
2 comprises a blocking transistor connected between a drain of
3 the output transistor and the first transistor, said blocking
4 transistor having a gate connected to a gate of the row select
5 transistor.

1 9. The imaging device of claim 1, further comprising a
2 gain selector to enable a change in gain in the amplifier.

1 10. The imaging device of claim 3, further comprising a
2 gain selector to enable a change in gain in the amplifier,
3 said gain selector comprising:

4 a first gain transistor having a drain connected to the
5 first voltage source; and

6 a first gain-enable transistor connected between a source
7 of the gain transistor and the source of the first transistor,
8 wherein while the first gain-enable transistor is
9 conducting, the first transistor and the first gain transistor
10 are connected in parallel.

1 11. The imaging device of claim 10, wherein the gain
2 selector further comprises:

3 a second gain transistor having a drain connected to the
4 first voltage source; and

5 a second gain-enable transistor connected between a
6 source of the second gain transistor and the source of the
7 second transistor,

8 wherein while the second gain-enable transistor is
9 conducting, the second transistor and the second gain
10 transistor are connected in parallel.

1 12. The imaging device of claim 10, wherein each of the
2 first gain transistor and the first gain enable transistor is
3 p-type transistor.

1 13. An imaging device comprising:

2 a plurality of active pixel sensor cells, each
3 having a photosensor, a row select transistor, and an output
4 transistor including a gate connected to a pixel output
5 voltage; and

6 a readout circuit connectable to each of said APS
7 cells, said readout circuit including an amplifier, said
8 amplifier comprising:

9 a first branch comprising:

10 a first transistor having a drain connected to
11 a first voltage source;

12 the row select transistor of each pixel; and

13 the output transistor of each pixel;
14 a second branch comprising:
15 a second transistor having a drain connected to
16 the first voltage source;
17 a third transistor having a gate connected to a
18 second voltage source;
19 a fourth transistor; and
20 a source follower transistor having a drain
21 connected to a source of each of the fourth
22 transistor and the output transistor of each pixel.

1 14. The imaging device of claim 13, wherein the
2 amplifier provides a gain of about one or higher.

1 15. The imaging device of claim 3, wherein the first
2 voltage source comprises V_{DD} .

1 16. The imaging device of claim 13, wherein each of said
2 transistors comprise a MOSFET.

1 17. The imaging device of claim 3, wherein each of the
2 first and second transistors comprise a p-type transistor and
3 each of the row select transistors, output transistors, third
4 transistor, fourth transistor, and source follower transistor
5 comprise an n-type transistor.

ABSTRACT

An active pixel sensor (APS) includes an array of individually addressable APS cells and a pixel readout structure that includes an amplifier. The amplifier may have a two-branched structure and provide a gain of one or higher. Additional switches may be provided in the pixels to provide protection for pixel output transistors from voltage changes in the column line. Structure may also be provided for optional gain selection in the amplifier.

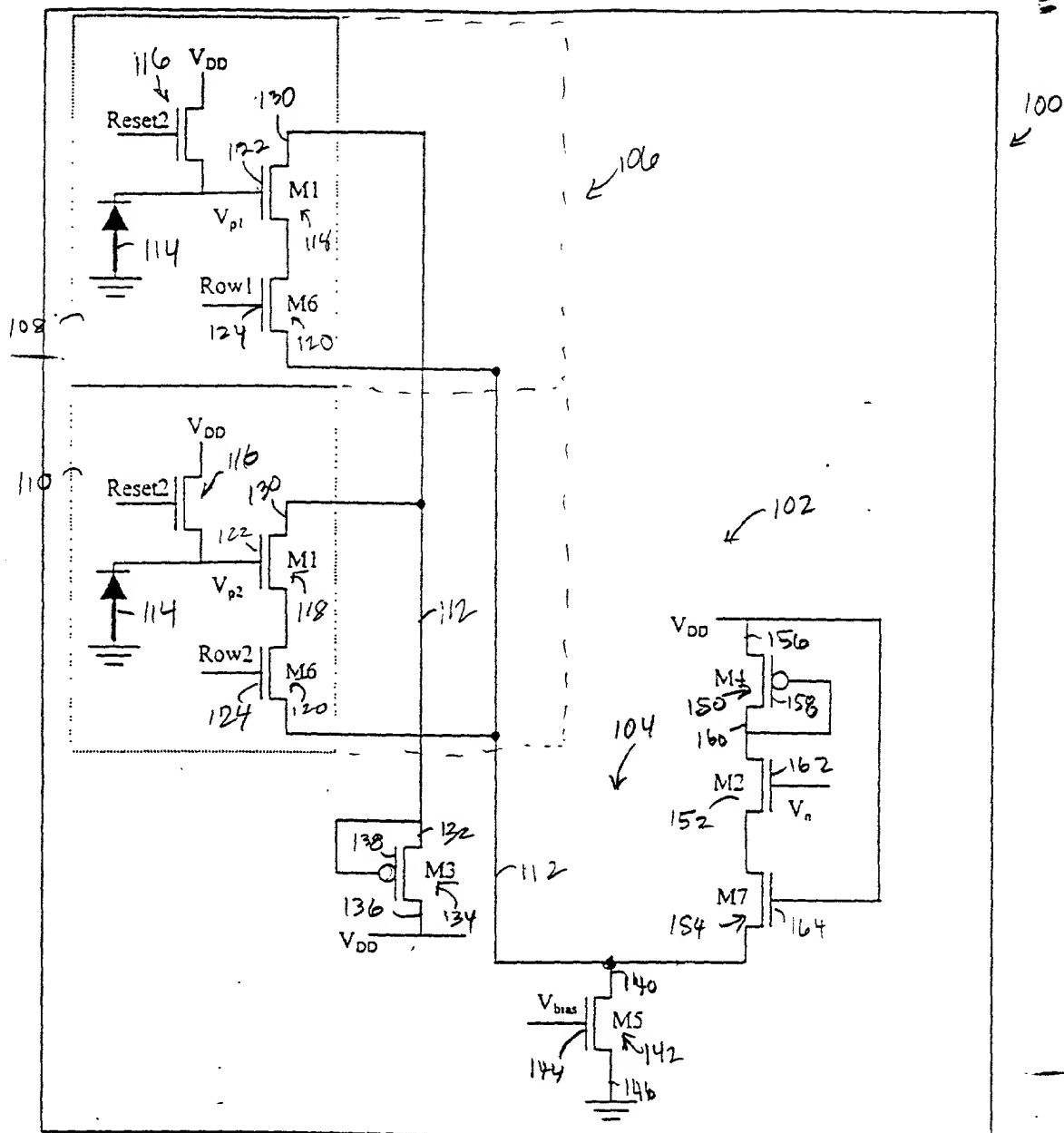


Figure 1. The new readout structure

FIG. 1

APPENDIX A

How to build a preamplifier

A typical preamplifier is shown in Figure 2.

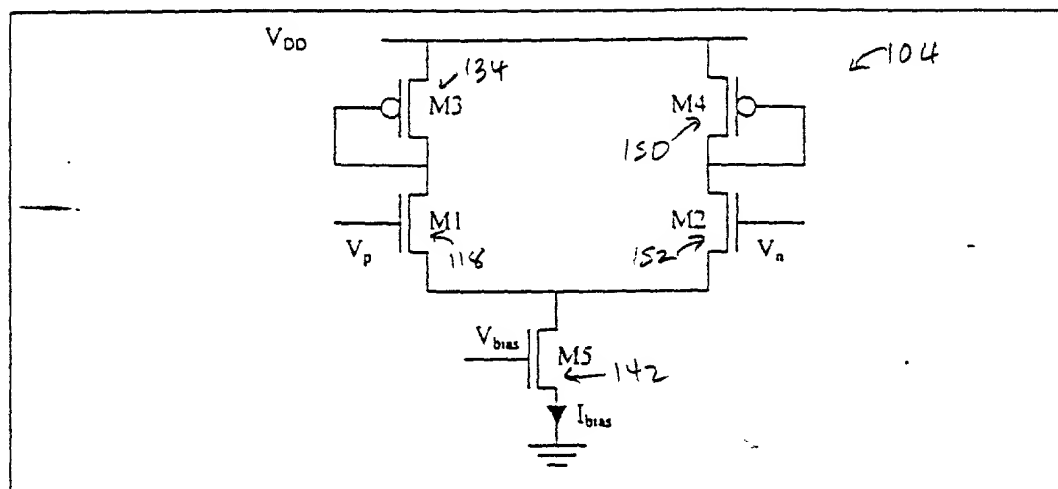


Figure 2. Schematics of a typical preamplifier

FIG 2



Photobit

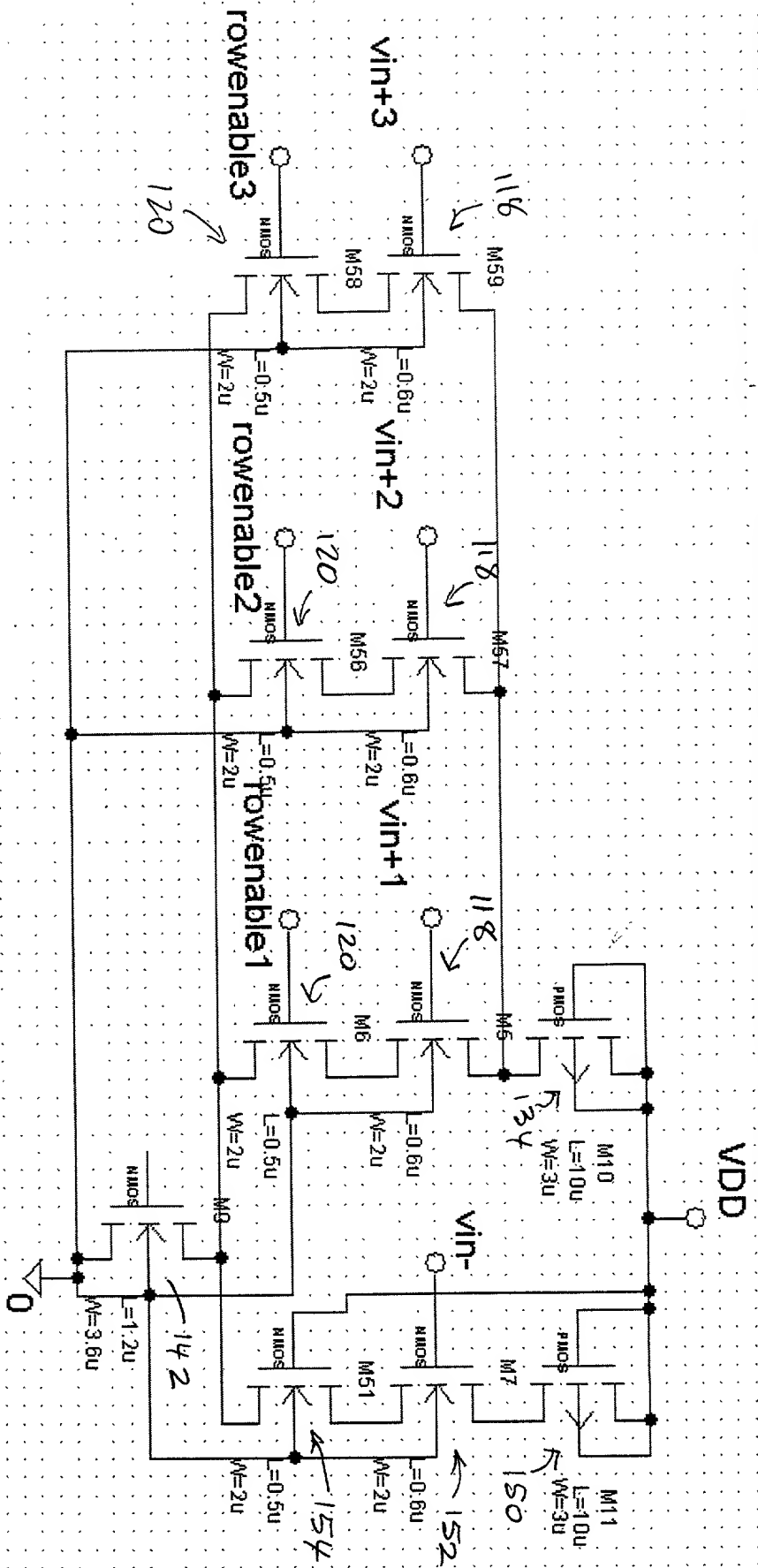


FIG. 3

Leading the Active Pixel Revolution

0059592 061500

(A) readoutnovel2.dat

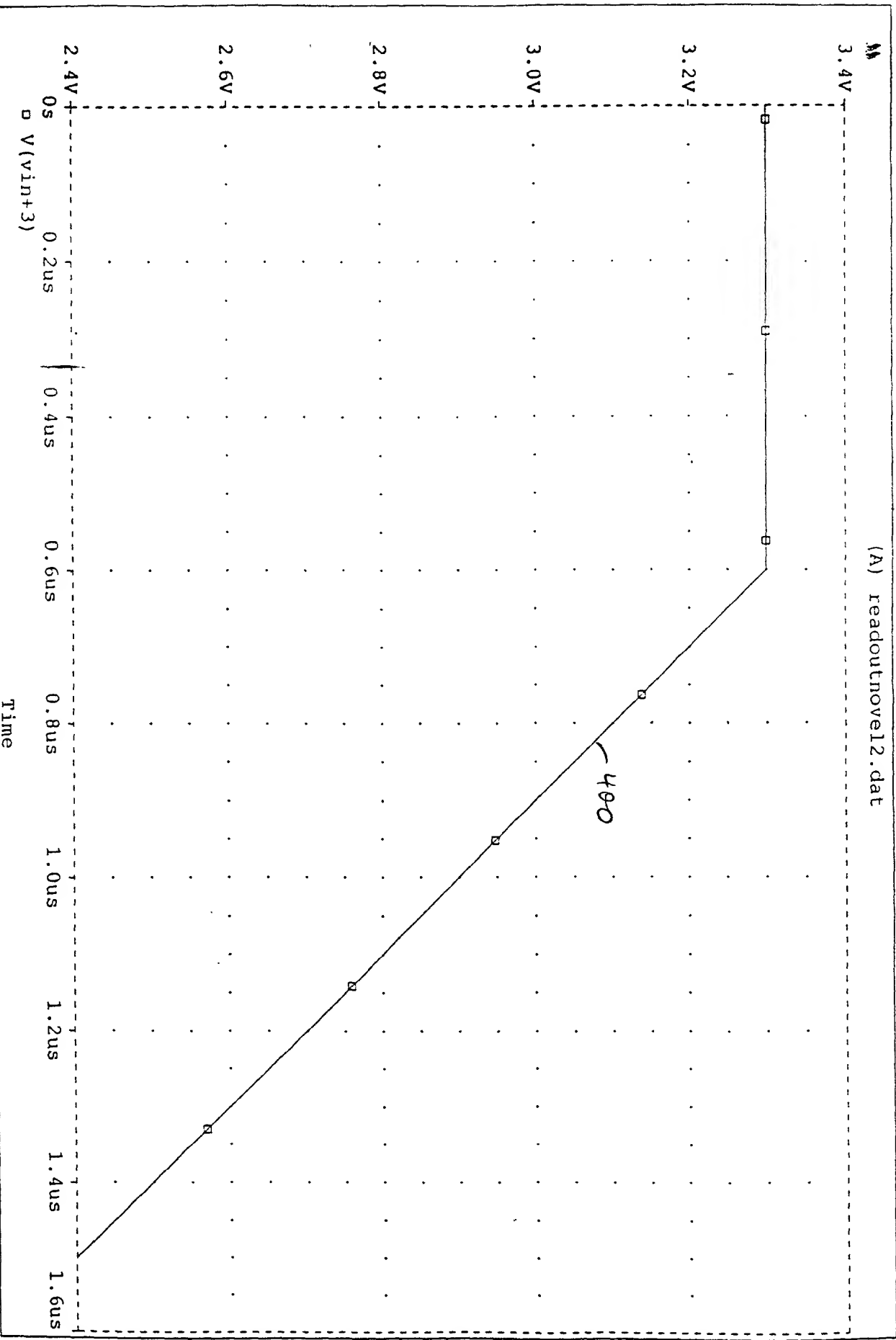
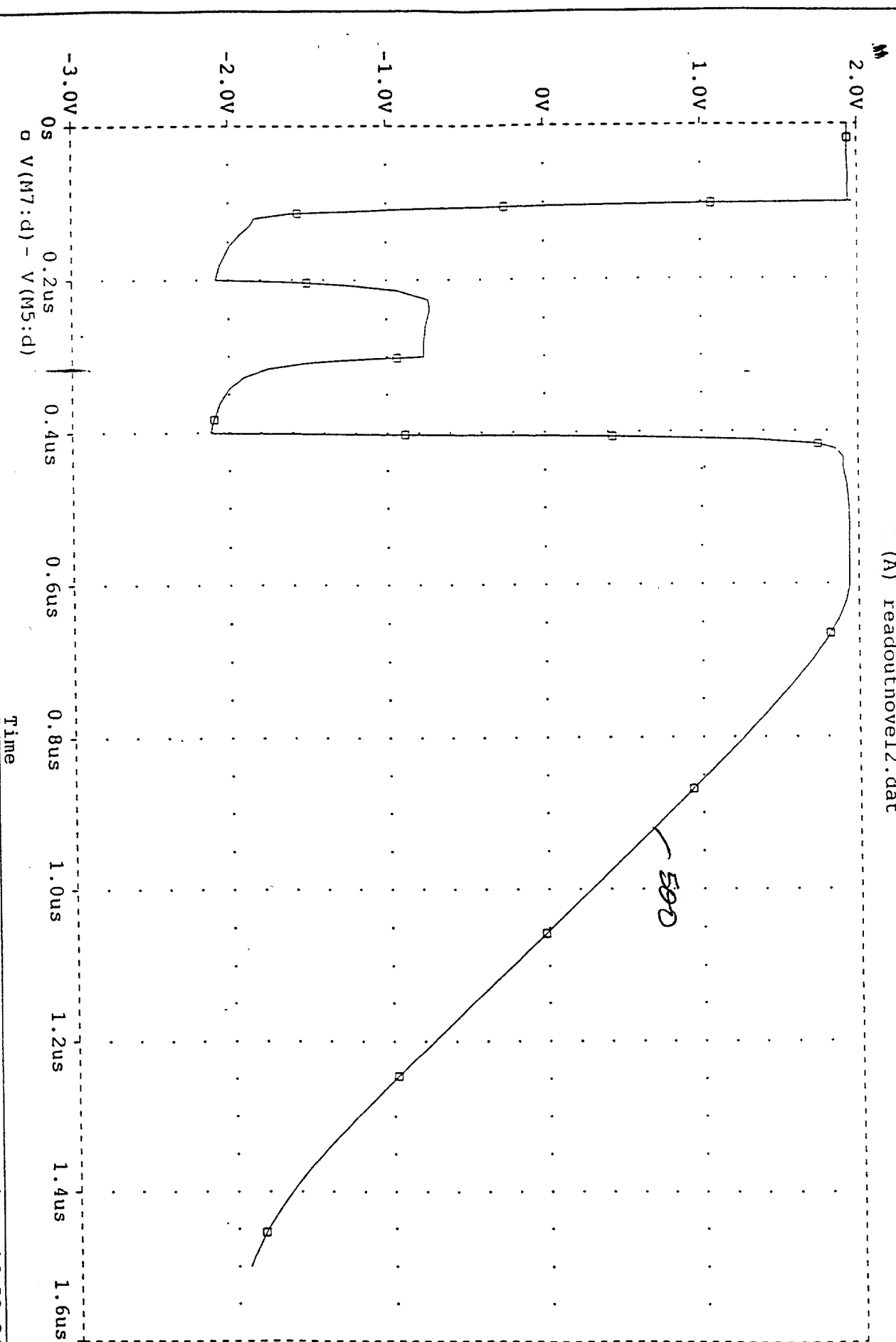


FIG. 4

(A) readoutnovel2.dat



FBI

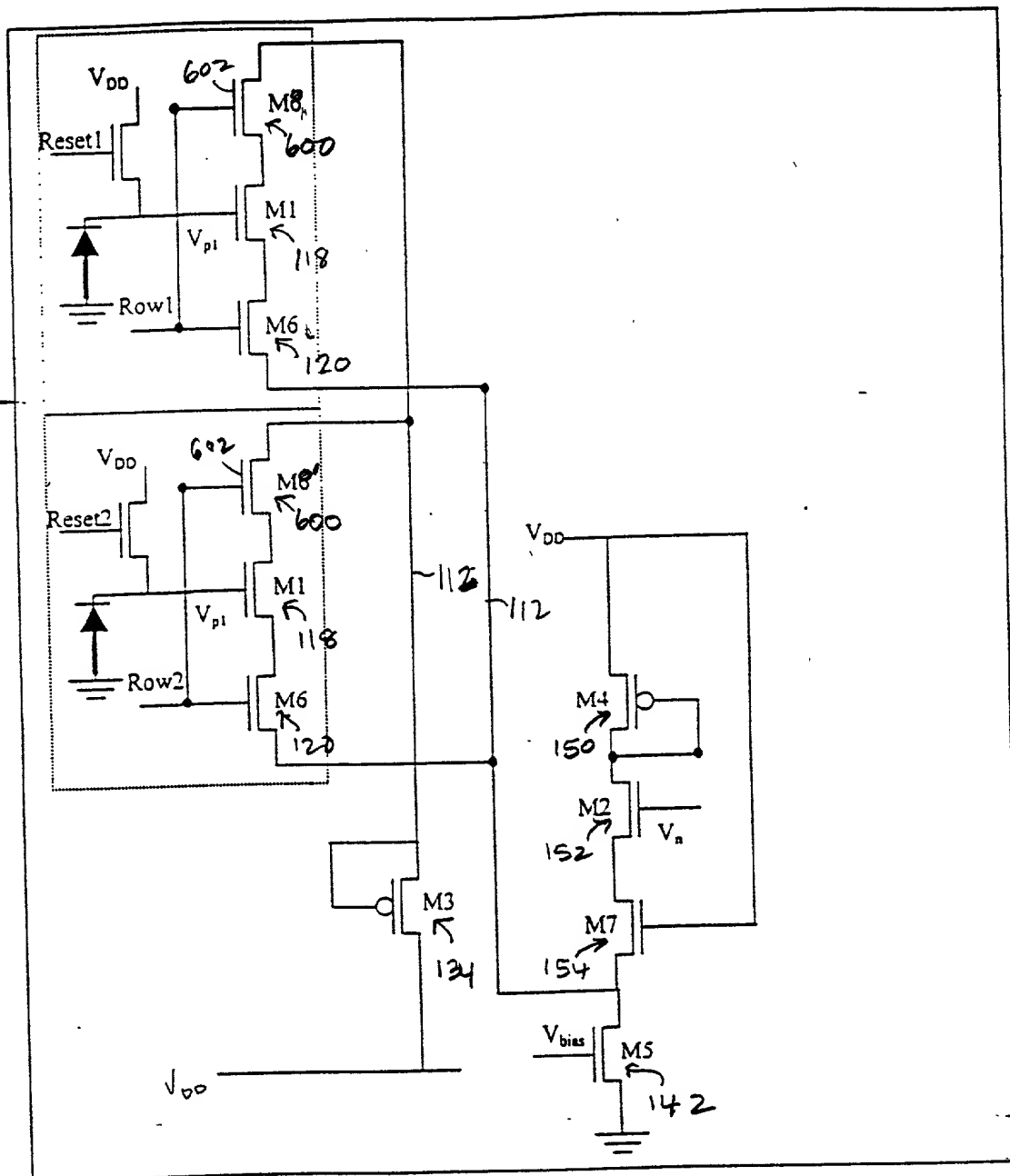


Figure 1. Amplifier readout with minimum effect from the column output.

FIG. 6

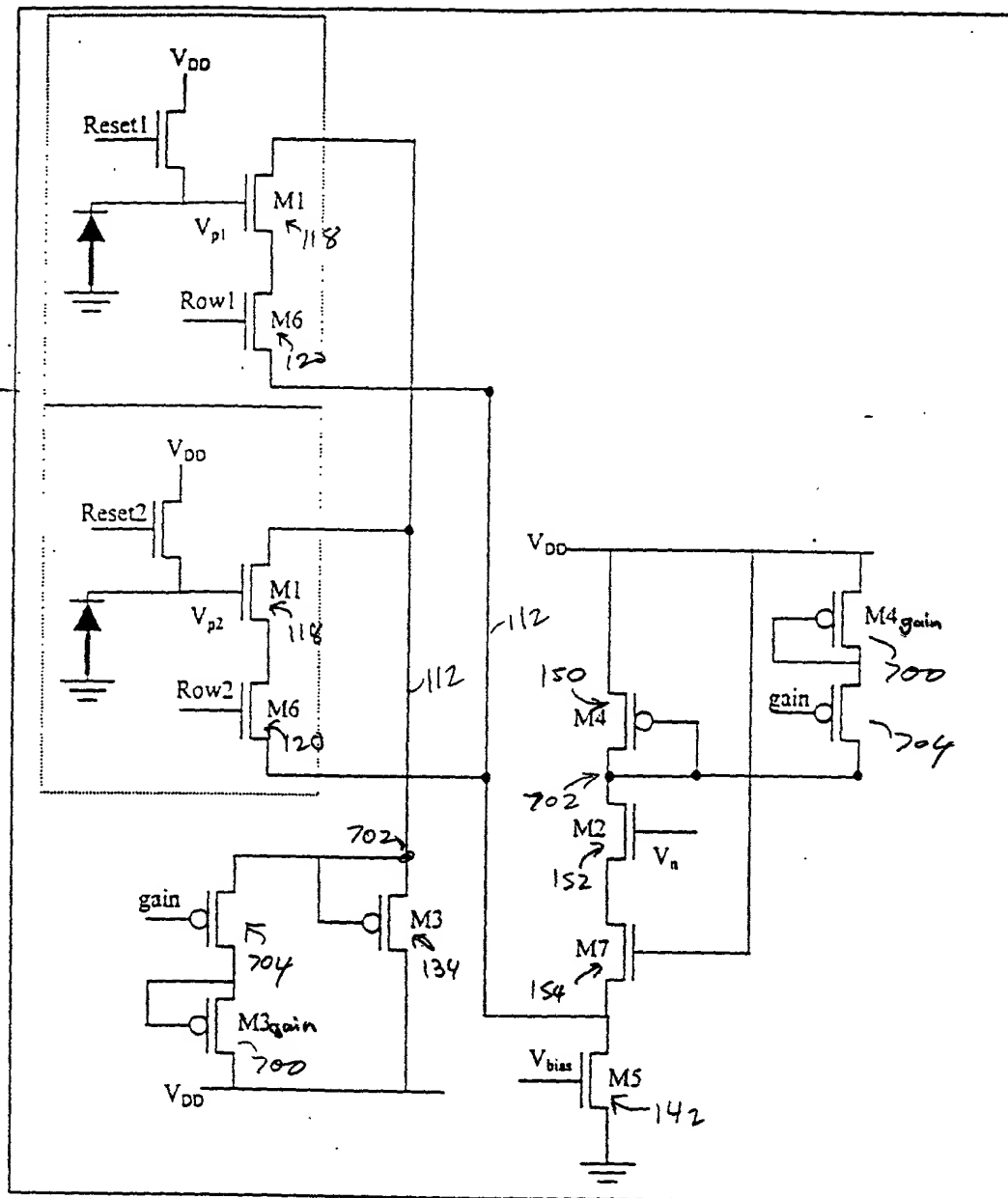


Figure 1. The new readout structure with different gain settings

FIG. 7,

COMBINED DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled ACTIVE PIXEL SENSOR (APS) READOUT STRUCTURE WITH AMPLIFICATION, the specification of which:

☒ is attached hereto.

☐ was filed on _ as Application Serial No. _ and was amended on _____.

☐ was described and claimed in PCT International Application No. _____ filed on _____ and as amended under PCT Article 19 on _____.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose all information I know to be material to patentability in accordance with Title 37, Code of Federal Regulations, §1.56.

I hereby claim the benefit under Title 35, United States Code, §119(e)(1) of any United States provisional application(s) listed below:

U.S. Serial No.	Filing Date	Status
60/139,348	June 15, 1999	Pending

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose all information I know to be material to patentability as defined in Title 37, Code of Federal Regulations, §1.56(a) which became available between the filing date of the prior application and the national or PCT international filing date of this application:

U.S. Serial No.	Filing Date	Status
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I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate or of any PCT international application(s) designating at least one country other than the United States of America listed below and have also identified below any foreign application for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date before that of the application(s) of which priority is claimed:

Country	Application No.	Filing Date	Priority Claimed
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Attorney Docket No.: 08305/073001/99-08/99-09/99-10

Combined Declaration and Power of Attorney
Page 2 of 2 Pages

I hereby appoint the following attorneys and/or agents to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

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David L. Feigenbaum, Reg. No. 30,378
Hans R. Troesch, Reg. No. 36,950
Bing Ai, Reg. No. 43,312
Samuel L. Lee, Reg. No. 42,791
Frederick H. Rabin, Reg. No. 24,488

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that those statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patents issued thereon.

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